Japanese Patent Laid-Open No. 57-10975

Applicant: Sanyo Electric Co., Ltd.

Specification

1. Title of the Invention:

MOS Transistor having High Dielectric Strength

2. Claim:

1. An MOS transistor comprising:

a second conduction type source region and a second conduction type drain region which are formed in comb shapes apart from each other on a first conduction type semiconductor substrate;

a second conduction type low impurity concentration region formed on a side of said drain region; and

a channel region which is formed between said low impurity concentration region and said source region, characterized in that the low impurity concentration region is configured so as to have a length as measured from a tip of said comb shaped drain region to said channel region which is longer than other portions.

3. Detailed Description of the Invention:

The present invention relates to a structure of an MOS transistor which has high dielectric strength to a drain voltage.

Since an MOS transistor generally has a switching speed far higher than that of a bipolar transistor and exhibits an input characteristic having a positive coefficient, it is used mainly as a high-frequency element or a power element.

Figure 1 shows a sectional structure of an ordinary MOS transistor. In Figure 1, a reference numeral 1 represents a P type silicon substrate, reference numerals 2 and 3 designate an N^+ conduction type source region and an N^+ conduction type drain region respectively, a reference numeral 4 denotes a gate oxide film, and reference numerals 5, 6 and 7 represent a source electrode, a drain electrode and a gate electrode respectively. Furthermore, dashed lines shown in Figure 1 are equipotential lines which are formed when a drain voltage is applied. Though dielectric strength to a drain voltage is limited by dielectric strength of a junction between the drain region 3 and the substrate 1, it is actually determined, as apparent from the equipotential lines, depending on concentration of an electric current in the vicinity of a surface of the drain region 3 which is caused due to overlapping between the gate electrode 7 and the drain region 3 and the dielectric strength is only on the order of 50 V when the gate oxide film 4 is on the order of 1000Å.

A sectional structure of an MOS transistor which has enhanced dielectric strength to a drain voltage is shown in Figure 2, wherein a reference numeral 8 represents a P type silicon substrate, reference numerals 9 and 10 designate an N^+ conduction type source region and an N^+ conduction type drain region respectively, reference numerals 11, 12 and 13 denote a source electrode, a drain electrode and a gate electrode respectively, and an N^- type low impurity concentration

region 15 is disposed in a direction from the drain region 10 toward a channel region 14. Formation of this low impurity concentration region 15 extends the equipotential lines toward the channel region 14 as indicated by dashed lines, thereby preventing a current from being concentrated in the vicinity of a surface of the drain region 10 and enhancing dielectric strength to a drain voltage from 300 V to a level on the order of 400 V. This low impurity concentration region 15 is generally referred to as a drift channel.

On the other hand, a high transconductance can be obtained by shortening a gate length L and enlarging a gate width W as seen from $gm \propto W/L$ (W: gate width, L: gate length), but the gate length L cannot be extremely short and is usually set on the order of 2 to 7 μ. There is known a structure in which a source region and a drain regions are formed in shapes of combs to enlarge the gate width W. Figure 3 is a diagram partially showing a surface of an MOS transistor. In Figure 3, a reference numeral 16 represents a P type silicon substrate, reference numerals 17 and 18 designate an N^+ type source region and an N^+ type drain region respectively, a reference numeral 19 denotes an N^- type low impurity concentration region, a reference numeral 20 represents a channel region, and the source region 17 and the drain region 18 are formed in comb shapes and combined with each other. Accordingly, the channel region 20 is formed in a zigzag shape, thereby allowing the gate width to be enlarged. Since lines of electric force extend from a protruding tip of the drain region 18 as indicated by arrows, however, an electric current is concentrated on the tip, thereby making it conventionally impossible to enhance dielectric

strength to a drain voltage even when the low impurity concentration region 19 is formed.

The present invention which has been achieved in view of the point described above provides an MOS transistor which has a comb type structure correcting the conventional defect. The present invention will be described below with reference to the drawings.

Figure 4 is a view partially showing a surface of an embodiment of the present invention, wherein a reference numeral 21 represents a P type silicon substrate, reference numerals 22 and 23 designate an N^+ conduction type source region and an N^+ conduction type drain region respectively, a reference numeral 24 denotes an N^- conduction type low impurity concentration region, and a reference numeral 25 represents a channel region. A layer which has resistance Rs on the order of 10 to 20 Ωcm is used as the P type silicon substrate 21 and the low impurity concentration region 24 is formed by epitaxial growth or ion injection as a layer which has resistance Rs of 8 Ωcm and a depth on the order of 20 μ. On the other hand, the source region 22 and the drain region 23 are formed by dispersion in the comb shapes which are combined with each other, and the channel region 25 which contains a P type impurity which is injected by ion injection while controlling it to a predetermined channel concentration having a length of 3 μ and a width of 120 mm.

Furthermore, a length l of the low impurity concentration region 24 is formed so as to reserve a distance between the drain region 23 and the channel region 25, or have a length l on the order of 60 μ, but a length l' of the low impurity concentration region 24 as measured from a tip of the drain region 23 to the channel region 25 is longer

than that of other portions. That is, $l < l'$ is selected to prolong the lines of electric force extending from the tip to the channel region 25, thereby weakening an electric field in a section from the tip to the channel region 25 and enabling to prevent the concentration of the electric field.

Figure 5 shows a result which was obtained by experimental determination of a relationship between the length l' of the low impurity concentration region 24 and dielectric strength to a drain voltage. Dielectric strength to drain voltage V_{DSS} was 300 V at $l' = l$, 390 V at $l' = 1.5\ l$, 450 V at $l' = 2\ l$ and 465 V at $l' = 3\ l$. As apparent from the result shown in Figure 5, it is possible to enhance dielectric strength to a drain voltage to 400 V by forming l' at least $1.6\ l$ thereby obtaining a transistor which has dielectric strength remarkably higher than that of the conventional transistor.

As understood from the foregoing description, the present invention makes it possible to prevent an electric current from being concentrated and remarkably enhance dielectric strength to a drain voltage by configuring the low impurity concentration region so as to have a length as measured from the tip of the drain region to the channel region which is longer than that of other portions.

4. Brief Description of the Drawings:

Figure 1 is a partial sectional view showing a conventional example, Figure 2 is a partial sectional view showing an improved conventional example, Figure 3 is a front view of a conventional MOS transistor, Figure 4 is a front view illustrating an embodiment of the present invention, and Figure 5 is a graph illustrating a

relationship between dielectric strength to a drain voltage V_{DSS} and a length l' of a low impurity concentration region.

21 ... P type silicon substrate, 22 ... Source region, 23 ... Drain region, 24 ... Low impurity concentration region, 25 ... Channel region.

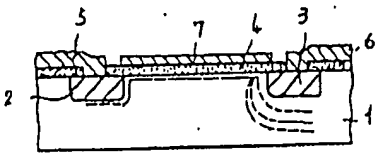
Applicant: Sanyo Electric, Co., Ltd., and one other person

Agent: Patent Attorney; Shizuo Sano

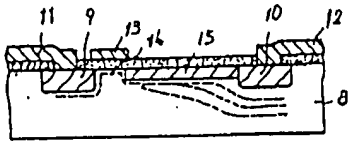
Figure 5

#1 Length of l'

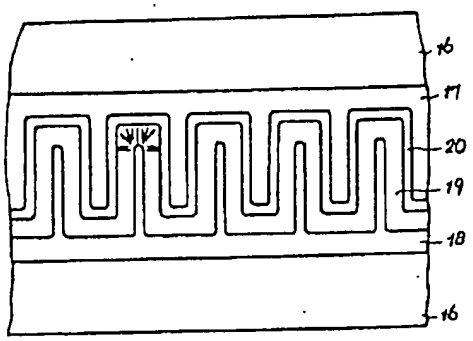
第1図



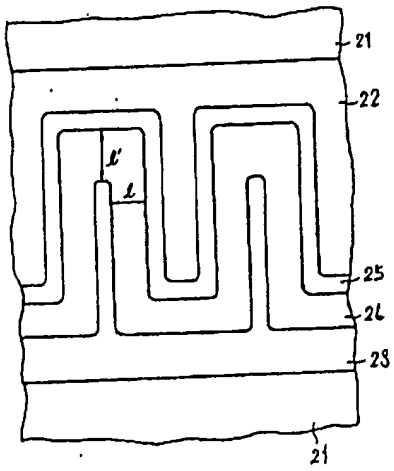
第2図



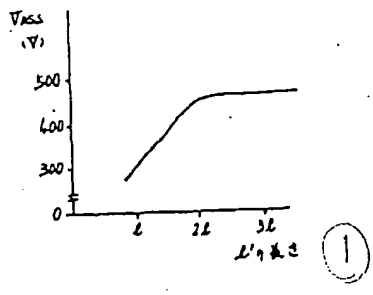
第3図



第4図



第5図



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⑤4高耐圧MOSトランジスタ

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㉒発 明 者 田中忠彦
群馬県邑楽郡大泉町大字坂田180番地東京三洋電機株式会社内
㉒発 明 者 野崎勉
群馬県邑楽郡大泉町大字坂田180番地東京三洋電機株式会社内
㉑出 願 人 三洋電機株式会社
守口市京阪本通2丁目18番地
㉑出 願 人 東京三洋電機株式会社
群馬県邑楽郡大泉町大字坂田180番地
㉔代 理 人 弁理士 佐野静夫

明　細　書

1. 発明の名称　高耐圧MOSトランジスタ

2. 特許請求の範囲

1. 第1導電型半導体基体上に互いに離れて島形に形成された第2導電型のソース、ドレイン領域と、該ドレイン領域側に形成された第2導電型の低不純物濃度領域と、該低不純物濃度領域と前記ソース領域との間に形成されたチャンネル領域とを備え、前記島形のドレイン領域の先端部と前記チャンネル領域までの低不純物濃度領域の距離を他の部分より長く形成したことを特徴とする高耐圧MOSトランジスタ。

3. 発明の詳細な説明

本発明はドレイン耐圧の高いMOSトランジスタの構造に関する。

一般にMOSトランジスタはスイッチングスピードがバイポーラトランジスタに比べて非常に早く、入力特性が正の係数を持っている為主に高周波素子及びパワー用素子として用いられる。

通常のMOSトランジスタの断面構造を第1図に示す。第1図に於いて、(1)はP型シリコン基板、(2)(3)はそれぞれN^+導電型を有するソース、ドレイン領域、(4)はゲート酸化膜、(5)(6)(7)はそれぞれソース電極、ドレイン電極、ゲート電極を示す。また第1図中に示された破線はドレイン電圧を印加した場合の等電位線である，ドレイン耐圧はドレイン領域(3)と基板(1)との接合耐圧で制限されるが、実際には等電位線から明らかな様に、ゲート電極(7)とドレイン領域(3)との重なりに依って生じるドレイン領域(3)表面近傍の電流集中に依って決定され、ゲート酸化膜(4)が1000Å程度の場合にはドレイン耐圧は50V程度にしかならない。

第2図はドレイン耐圧を向上させたMOSトランジスタの断面構造であり、(8)はP型シリコン基板、(9)(10)はそれぞれN^+導電型のソース、ドレイン領域、(11)(12)(13)はそれぞれソース電極、ドレイン電極、ゲート電極であり、ドレイン領域(10)からチャンネル領域(14)方向にN^-型の低不純物濃度領域(15)が設けられている。この低不純物濃度領域(15)を形成することに依り、等電位線は破線で示される